Claims

[c1] 1. A method of testing an integrated circuit, said method comprising:
scanning in a plurality of bits sequentially on a pin, said plurality of bits forming a test code which indicates the specific ones of a plurality of tests to be performed; and
performing said specific ones of said plurality of tests in parallel.

[c2] 2. The method of claim 1, wherein each of said plurality of bits indicates whether a corresponding one of said plurality of tests is to be performed.

[c3] 3. The method of claim 2, further comprising:
shifting in said plurality of bits into a shift register; and
loading said plurality of bits from said shift register to a second register, wherein a bit value in each bit of said second register determines whether a corresponding one of said plurality of tests is to be performed.

[c4] 4. The method of claim 3, wherein said shifting and said performing are performed in parallel.

[c5] 5. The method of claim 4, wherein said scanning scans a plurality of control bits on said pin, said plurality of con-

trol bits representing control signals associated with said plurality of tests.

[c6] 6. The method of claim 5, wherein said scanning scans some bits of said test code on a first pin and some other bits of said test code on a second pin, wherein said pin corresponds to one of said first pin and said second pin.

[c7] 7. A tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block being contained in said integrated circuit, said tests enabler block comprising:
a first pin receiving a plurality of bits sequentially, said plurality of bits forming a test code which indicates the specific ones of a plurality of tests to be performed to test said integrated circuit.

[c8] 8. The tests enabler block of claim 7, wherein each of said plurality of bits indicates whether a corresponding one of said plurality of tests is to be performed.

[c9] 9. The tests enabler block of claim 8, further comprising a first storage element storing said plurality of bits, wherein a bit value in each bit of said first storage element determines whether a corresponding one of said plurality of tests is to be performed.

[c10] 10. The tests enabler block of claim 9, further comprises

a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin.

[c11] 11. The tests enabler block of claim 10, wherein said first storage element comprises a first register, wherein said plurality of bits are loaded from said shift register to said first register.

[c12] 12. The tests enabler block of claim 11, further comprises:
a second pin receiving a status signal indicating whether said integrated circuit is to be operated in a test state or a functional state;
a plurality of phase pins receiving a plurality of phase signals, wherein said plurality of phase signals operate said shift register in a shift phase in which said plurality of bits are scanned into said shift register, said plurality of phase signals operate said first register in a load phase in which said plurality of bits are loaded from said shift register to said first register.

[c13] 13. The tests enabler block of claim 12, wherein a new plurality of bits are scanned sequentially into said shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed.

[c14] 14. The tests enabler block of claim 13, wherein said first pin receives a plurality of control bits sequentially, said plurality of control bits representing control signals associated with said plurality of tests.

[c15] 15. The tests enabler block of claim 14, wherein some bits of said test code are scanned in on a third pin and some other bits of said test code are scanned in on a fourth pin, wherein said first pin corresponds to one of said third pin and said fourth pin.